REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-30 previously presented for examination remain in the application. Claims 18, 19 and 30 have been amended to correct typographical errors. No new claims have been added and no claims have been canceled.

The Specification has been amended as indicated to correct minor informalities.

Claims 1-3, 9-13, 19-23, 29 and 30 stand rejected under 35 U.S.C. § 102(b) as being considered to be anticipated by U.S. Patent No. 6,016,548 to Nakamura et al. ("Nakamura").

Claim 1 includes the limitations

> determining a processor state of a processor upon expiration of a system management interrupt (SMI) timer, the processor state being one of an operational state and a low power state;
> loading the SMI timer with a timer value based on the processor state, the timer value being one of a first value and a second value; and
> transitioning the processor to one of the operational state and the low power state according to the processor state.

(Claim 1)(emphasis added)

Applicant respectfully submits that Nakamura does not teach or suggest the claimed features of applicant's invention including at least determining a processor state of a processor upon expiration of a system management interrupt timer.

Nakamura discloses an apparatus for controlling duty ratio of power saving of CPU. It is stated in the Office Action that Nakamura discloses determining the processor state of a processor upon expiration of a system

management interrupt timer at column 2, lines 45-54. Applicant respectfully disagrees with this characterization of Nakamura. Instead, this passage refers to monitoring various hardware interrupt request signals (not a System Management Interrupt) to the CPU generated in the computer system and detecting a system idel when all of the hardware interrupt request signals are not generating for a predetermined time out period and means for supplying an interrupt signal indicating a system idle to the predetermined interrupt input terminal of the CPU in response to detection of the system idel by the system idel detecting means.

For at least this reason, Nakamura cannot be considered to teach the claimed features of applicant's invention. Further Nakamura does not suggest such a feature.

Independent claims 11 and 21 include a similar limitation. Claims 2-10, claims 12-20 and claims 22-30 depend from and further limit claims 1, 11 and 21, respectively and thus, should also be found to be patentably distinguished over Nakamura for at least the same reasons.

New claim 31 includes a limitation of determining whether throttling is enabled, which is also not disclosed by Nakamura. New claims 32-35 depend from and further limit claim 31 and thus, are also patentably distinguished over Nakamura.

Claims 4-8, 14-18 and 24-28 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Based on the foregoing, applicant respectfully submits that the applicable objections and rejections have been overcome and claims 1-35 are in condition for allowance.

If the Examiner disagrees or believes that further discussion will expedite prosecution of this case, the Examiner is invited to telephone applicant's representative Cynthia Thomas Faatz at (408) 765-2057.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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